Wirebonding for the SZOSS

From bare die to working chip on a board

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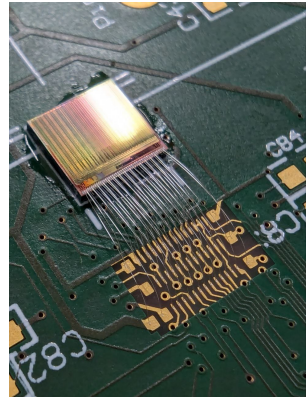
What is Chip-on-Board?

You taped out on a shuttle. Some months later the **bare dies** come back. Now they need to talk to the outside world.

Chip-on-Board (CoB)

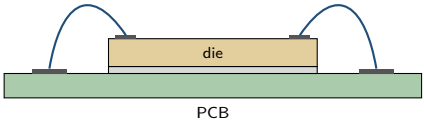
- Bare die glued directly onto the PCB (**die attach**)
- Chip pads connected to board pads (**bond fingers**)
- No package: cheaper, smaller, shorter connections
- Direct access to special pads, probe points, sensors
- **But: no standard footprint.** You design it for every chip.

Packaged (QFN, QFP, . . .): standard footprint, but cost, lead time, extra inductance and a fixed pinout.

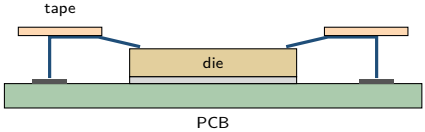


A bare die on a test PCB, wires fanning out to the bond fingers.

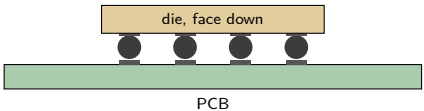
Different ways to connect die and board



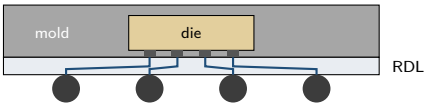
Wire bonding: die glued first, then thin wires from die pads to board pads (wedge or ball)



TAB (tape automated bonding): metal leads on a flexible tape connect die and board



Flip-chip: die face down, bumps touch the board pads, no wires

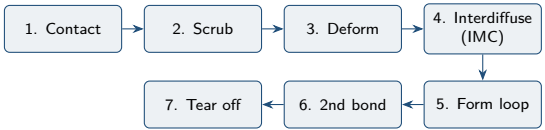


FOPLP: dies in a panel, redistribution layers fan the pads out to solder balls

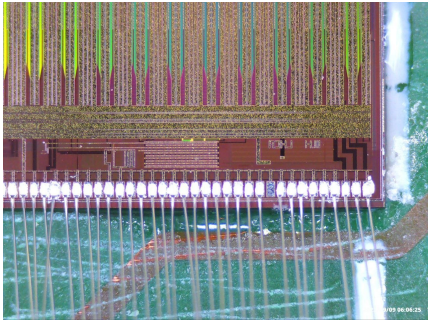
Wire bonding is the one a lab or a hackerspace can actually do: a used manual bonder starts around $25k, a new CNC bonder above $150k.

Wire bonding: an ultrasonic weld at room temperature

Tool presses an Al, Au or Cu wire onto the pad and vibrates it (60–140 kHz). Oxides break, clean metal meets clean metal, the atoms interdiffuse.



Parameter	Too low	Too high
Bond force	Non-stick on pad (NSOP)	Cratering, pad damage
Ultrasonic power	Poor scrubbing, NSOP	Wire necking, cratering
Bond time	Bond lift	Brittle IMCs, pad damage
Cleanliness	NSOP, bond lift	– no drawback



Aluminium wedge bonds on the pad row of a pixel readout chip.

Full details: *Poor Man's Introduction to Wire-Bonding*, KiCon Europe 2025 / KiCon Asia 2025.

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TAB: glue the die, connect it with a flex

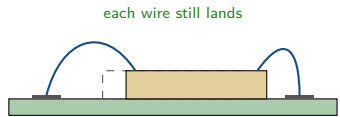
Tape automated bonding

- Copper leads on a flexible tape (or a flex PCB)
- All leads of a die are connected **in one step**, not wire by wire
- No loops: low inductance, low profile
- The lead pattern is defined once, by the flex design

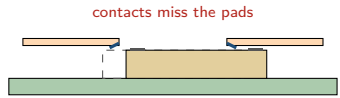
The catch: tolerances

Wires are placed one by one, so each wire follows the die where it really sits. A flex has a **fixed pattern**: if the die shifts during placement, **every contact** misses at once.

Wire bonding, die shifted



Flex / TAB, die shifted



Open question: which placement tolerance can a flex take? To be evaluated experimentally.

The challenge is not the bond, it is the board

1. The data is scattered

GDS, schematic, process documents, a slide. The copies drift apart.

2. Chicken and egg

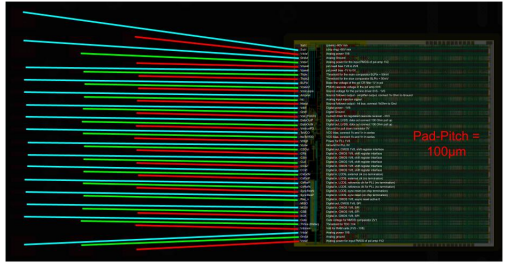
Wire length depends on the land pattern you are trying to design.

3. New chip, new footprint

Every chip iteration needs its own land pattern, drawn pad by pad.

4. Tolerances stay invisible

A die placed 50–100 μm off moves every wire landing point.

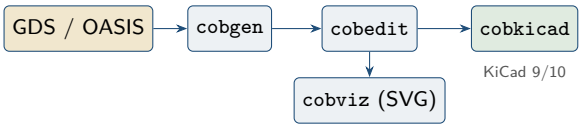


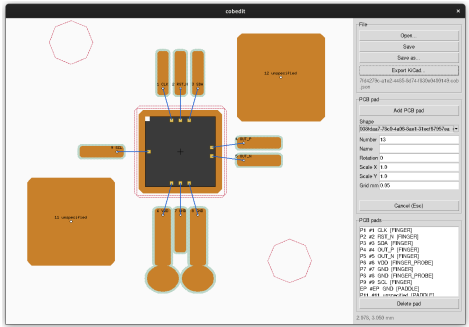
A typical bonding plan: a die photo, pad names and coloured lines on a slide. It works, but no tool can read it.

open.cob.json: describe the chip once, generate the rest

One open JSON file per die, between chip designer and PCB designer:

- `die`: size, notch, pads (from the GDS)
- `pcb`: pad shapes, pads, cutouts, fiducials
- `wires`: die pad to board pad, material, loop
- `assembly`, `tolerances`, `units`, `meta`
- `"unspecified"` = unknown, `"none"` = deliberately absent





Works today with **gf180mcu** and the wafer.space reticles.

Bring your chip and your PDK: run it through `cobgen` and tell me what broke.

github.com/MaxClerkwell/open.cob.json

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About me - Stephan Bökelmann



Need something special bonded? Hit me up and let's talk about it.

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Hire me and my team via nabla B engineering

Follow me for digital design, physics and ASICs

maxclerkwell.tech Instagram Xiaohongshu Discord

Extra: Design for Bonding

On the chip

- Pad openings large enough for the tool
  e.g. $\geq 70\,\mu$m for a 25 μm Al wedge
- Pads on the die edge, not in the middle of the die
- Top metallization decides wire, force and temperature: clarify it early
- Plan ground / substrate pads and extra probe pads
- A notch or marker, so the orientation is clear under the microscope

On the board

- Surface finish matching the wire
  e.g. Al wedge on ENIG
- Bond finger pitch and angle matching the pads; stagger when tight
- Short wires, equal length where it matters (EMC, differential pairs)
- Die attach area, via keepout under the die, fiducials
- Budget for placement tolerance: 50–100 μm

Not sure your chip or board fits this? **Bring it, let's talk.**

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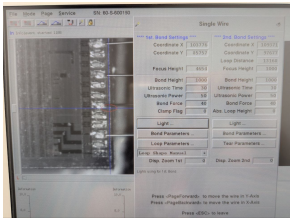
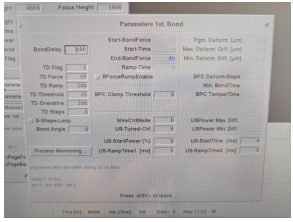
Extra: what a bonder program looks like

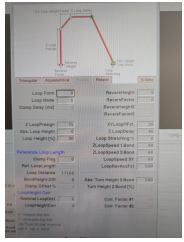
Every wire on the bonder needs its own set of parameters:



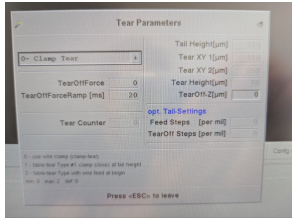
1. Placement



2. Bond: force, US, time



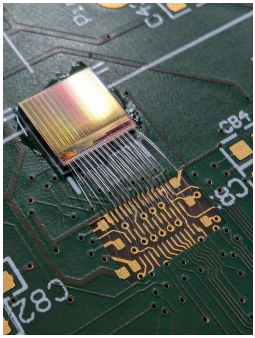
3. Loop trajectory



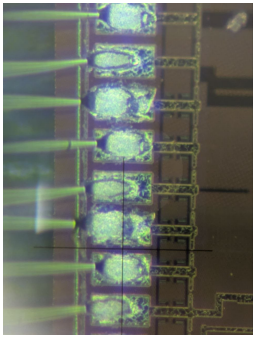
4. Tear off

- Placement comes from chip and board; bond and loop from wire, metallization and wire length
- All of this is already in a `*.cob.json` file
- **Next step for open.cob.json: generate the bonder program directly from the file**

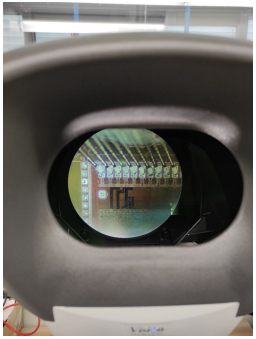
Extra: from the lab



Bare die glued and bonded on a test PCB



Bonded pixel chip under the microscope



What the bonder operator sees



Cleanroom, mask on

Two years of hands-on bonding of HV-MAPS detector chips. **Need something special bonded? Let's talk.**

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